Amendments to the Specification

Please amend the paragraph beginning on page 12, line 4, as follows:

Capacitor 29 is connected between output node N22 of level shift circuit 21 and output node N27 of level shift circuit 25. Capacitor 29 transmits potential changes of node N22 to node N27, and transmits potential changes of node N27 to node [[N27]] N22.

Please amend the paragraph beginning on page 14, line 14, as follows:

When drive circuit 20 is in the steady state, a through-current does not flow through pull-up circuit 30 and pull-down circuit 33, and the through-currents of level shift circuits 21 and 25 can be sufficiently reduced by sufficiently increasing the on-resistance values of resistance elements 22 and 26, as compared with the on-resistance values of transistors 23, 24, 26 and 27, so that the DC current can be reduced. Since capacitor [[26]] 29 is employed, it is possible to increase the responsivity to the changes in input potential VI.

Please amend the paragraph beginning on page 23, line 19, as follows:

In this third embodiment, since potential V22 of node N22 is boosted to a potential higher than the potential of (VI + |VTP| [[of]] $\pm$ VTN), which is to be originally achieved, in accordance with the rising of input potential VI from "L" level VL to "H" level VH, the rising rate of output potential VO can be increased. Since potential V27 of node N27 falls to the potential lower than the potential of (VI - |VTP| - VTN), which is to be originally achieved, in accordance with the lowering of input potential VI from "H" level VH to "L" level VL, the lowering rate of output potential VO can be increased. Therefore, the responsivity of drive circuit 75 can be increased.

Please amend the paragraph beginning on page 28, line 15, as follows:

Level shift circuit 111 is substantially the same as level shift circuit 96 except for that P-type transistors [[98]] 97 and 98 as well as N-type transistor 100 are eliminated, and N-type transistor 99 is connected between the source of P-type transistor 65 and node N22. A gate of N-type transistor 99 is connected to a drain of N-type transistor 99 and a gate of N-type transistor 101. Gate potential V99 of N-type transistors 99 and 101 is equal to (VI + |VTP| + 2VTN). N-type transistor 101 charges node N22 to a level of (V99 - VTN = VO + |VTP| + VTN).

Please amend the paragraph beginning on page 28, line 22, as follows:

Level shift circuit 112 is substantially the same as level shift circuit 102 except for that N-type transistors 103 and 104 as well as P-type transistor 105 are eliminated, and P-type transistor 106 is connected between node N27 and a drain of N-type transistor 70. P-type transistor 106 has a gate connected to its drain and a gate of P-type transistor 107. The gates of P-type transistors 106 and 107 are equal to (VI - VTN - 2VTP|). P-type transistor 107 discharges node N27 to (V106 + |VTP| = VI - VTN - |VTP|). Structures and operations other than the above are the same as those of drive circuit 95 in Fig. [[95]] 26, and therefore, description thereof is not repeated.

Please amend the paragraph beginning on page 31, line 12, as follows:

In the following description, it is assumed that an output potential of drive circuit 121 is lower than its input potential by offset voltage VOF. In the initial state, as shown in Fig. 34, all switches S1 - S4 are off. When switches S1 and S2 are turned [[off]] on at certain time t1, potential V20 of input node N20 of drive circuit 121 becomes equal to VI, and output potential

V30 of drive circuit 121 and a potential V122 of node N122 become equal to (VI - VOF) so that capacitor 122 is charged to offset voltage VOF.

Please amend the paragraph beginning on page 37, line 13, as follows:

A drive circuit 136 with the offset-compensating function shown in Fig. 43 is substantially the same as drive circuit 135 [[1]] with the offset-compensating function shown in Fig. 42 except for that N-type transistors 23 and 34 as well as P-type transistors 27 and 32 are eliminated. This modification can reduce an area occupied by the circuit.

Please amend the paragraph beginning on page 38, line 2, as follows:

A drive circuit 145 with the offset-compensating function shown in Fig. 46 is substantially the same as drive circuit 95 ~~with the offset-compensating function~~ shown in Fig. 26 except for that drive circuit 145 additionally includes an offset-compensating circuit formed of capacitors 122a, 122b, 126a and 126b as well as switches S1a - S4a and S1b - S4b. During a period between times t1 and t2 in Figs. 36 and 37, signal ϕB attains the "H" level in a pulse-like fashion, and signal /ϕB attains the "L" level in a pulse-like fashion. In this modification, potentials V22 and V27 of nodes N22 and N27 rapidly reach the predetermined values so that the operation speed can be high.

Please amend the paragraph beginning on page 46, line 18, as follows:

When output potential VO is higher than input potential VI, transistors 31 and 32 of pull-up circuit 30 are turned off, and transistors 34 and 35 of pull-down ~~transistor~~ circuit 33 are turned on so that output potential VO lowers. When output potential VO is lower than input potential

VI, transistors 34 and 35 of pull-down ~~transistor~~ circuit 33 are turned off and transistors 31 and 32 of pull-up circuit 30 are turned on so that output potential VO rises. Therefore, VO becomes equal to VI.

Please amend the paragraph beginning on page 53, line 13, as follows:

If drive circuit [[2224]] 224 and switches 226 and 229 were not employed, a leak current would flow between the gate of P-type transistor 222 and data line 6 through parasitic resistances of switches 225 and 227 so that the gate potential of P-type transistor 222 would change, and the brightness of EL element 220 would change.

Please amend the paragraph beginning on page 54, line 16, as follows:

When scanning line 4 falls to the ~~selected~~ unselected level of "L", switches 235 - 237 are turned off, and switches 238 and 239 are turned on. Since the gate potential of N-type transistor 232 is held by capacitor 233, gradation current IG flows from the line of power supply potential VCC to the line of ground potential GND through EL element 220, switch 238 and N-type transistor 232, and EL element 220 emits light at brightness corresponding to gradation current IG.